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ABSTRACT OF ~~THE DISCLOSURE~~

A semiconductor memory device includes first and second word lines which extend in parallel to each other, at least one line activation signal line which extends perpendicularly to the first and second word lines, a device isolation region which extends perpendicularly to the first and second word lines, a first driver for activating the first word line and ~~comprising~~ having a first impurity region provided adjacent to the device isolation region and connected to the word line activation signal line, a first gate electrode and a second impurity region connected to the first word line, a second driver for activating the second word line and comprising a third impurity region provided adjacent to the device isolation region on an opposite side from the first impurity region and connected to the word line activation signal line, a second gate electrode and a fourth impurity region connected to the second word line, and a decoder connected to the first and second gate electrodes.

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